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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/656,170	09/08/2003	Yoshiharu Hirakata	07977-241003	07977-241003 9943		
26171	7590 01/26/2004		EXAMINER			
	CHARDSON P.C.		NHU, E	NHU, DAVID		
1425 K STREET, N.W. 11TH FLOOR			ART UNIT	PAPER NUMBER		
WASHINGT	ON, DC 20005-3500		2818			
			DATE MAILED: 01/26/2004	1		

Please find below and/or attached an Office communication concerning this application or proceeding.

J		Applic	cation No.	Applicant(s)			
Office Action Summary		10/65	5,170	HIRAKATA ET AL			
		Exami	ner	Art Unit			
		David		2818			
Period fo	The MAILING DATE of this commu or Reply	nication appears on	the cover sheet with t	the correspondence ad	Idress		
THE I - External after - If the - If NO - Failu - Any r	ORTENED STATUTORY PERIOD MAILING DATE OF THIS COMMUN nsions of time may be available under the provision SIX (6) MONTHS from the mailing date of this comperiod for reply specified above is less than thirty period for reply is specified above, the maximum reto reply within the set or extended period for reply received by the Office later than three months ad patent term adjustment. See 37 CFR 1.704(b).	NICATION. as of 37 CFR 1.136(a). In n amunication. (30) days, a reply within the statutory period will apply as by will, by statute, cause the	o event, however, may a reply statutory minimum of thirty (30 nd will expire SIX (6) MONTHS application to become ABANE	be timely filed 0) days will be considered time 5 from the mailing date of this of	ly. ommunication.		
1)🛛	Responsive to communication(s) fi	led on <u>08 Se<i>ptemb</i></u>	<u>er 2003</u> .				
2a) <u></u> □	This action is FINAL.	2b)⊠ This action i	s non-final.				
3)	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Dispositi	ion of Claims						
5)□ 6)⊠ 7)□	Claim(s) 1-99 is/are pending in the 4a) Of the above claim(s) 1-55 is/are Claim(s) is/are allowed. Claim(s) 56-99 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restr	e withdrawn from c					
	ion Papers		·				
9)[The specification is objected to by t	he Examiner.					
10)	The drawing(s) filed on is/ar	e: a)∐ accepted o	r b)□ objected to by	the Examiner.			
	Applicant may not request that any obj						
	Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
•	The oath or declaration is objected	to by the Examiner	. Note the attached O	ffice Action or form P	10-152.		
•	under 35 U.S.C. §§ 119 and 120						
* 5 13)	Acknowledgment is made of a claim All b) Some * c) None of: 1. Certified copies of the priorit 2. Certified copies of the priorit 3. Copies of the certified copies application from the Internat See the attached detailed Office act Acknowledgment is made of a claim ince a specific reference was included a comparation of the foreign in the translation of the foreign incerence was included in the first see the seed of the comparation of the foreign incomparation.	y documents have y documents have s of the priority docional Bureau (PCT ion for a list of the confor domestic prioritied in the first sente anguage provisional for domestic priorities.	been received. been received in Appl uments have been rec Rule 17.2(a)). certified copies not rec y under 35 U.S.C. § 1 ence of the specification application has been y under 35 U.S.C. §§ fication or in an Appli	lication No. 09/730,41 ceived in this National ceived. 119(e) (to a provisional on or in an Application received. 120 and/or 121 since cation Data Sheet. 37	I Stage al application) a Data Sheet. e a specific 7 CFR 1.78.		
Attachmen	ut(s)		X	mi Du	-		
2) Notic	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review mation Disclosure Statement(s) (PTO-1449)			nmary (PTO-413) Paper No rmal Patent Application (PT			

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DETAIL ACTIONS

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 56-99 are rejected under U.S.C 103(a) as being unpatentable Background of Invention (BOI) in view of Majima et al (5,592,318).

Regarding claims 56, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: planaring an insulating film formed over a substrate 205 having an isulating surface; forming electrodes 206 on the insulating film; forming an insulating layer so as to cover the electrodes.

BOI fails to teach planarizing surfaces of the electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other, thereby filling boundary portions between the electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 57-59, see BOI, page 1-3, Majima, col. 1-12.

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It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes. Regarding claim 60, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: planaring an insulating film formed over a first substrate 205 having an isulating surface; forming stripped electrodes 206 on the insulating film; forming an insulating layer so as to cover the electrodes.

BOI fails to teach planarizing surfaces of the stripped electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the stripped electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the stripped electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other, thereby filling boundary portions between the stripped electrodes with the insulating layer (see col. 10, lines 13-32).

Regarding claims 61-63, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the Application/Control Number: 10/656,170

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same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes. Regarding claims 64, 69, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: forming semiconductor elements 206, 207 over a substrate 205 having an insulating surface; forming an interlayer insulating film over the semiconductor elements; planaring the interlayer insulating film; forming pixel electrodes 208, 209 that arte electrically connected to the respective semiconductor elements on the interlayer insulating film; forming an insulating layer so as to cover the pixel electrodes. BOI fails to teach planarizing surfaces of the pixel electrodes and a surface of the insulating layer so that they become flush with each other, thereby filling boundary portions between the

pixel electrodes with the insulating layer. However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the step of planarizing surfaces of the pixel

electrodes 4 and a surface of the insulating layer 5 so that they become flush with each other,

thereby filling boundary portions between the pixel electrodes with the insulating layer (see col.

10. lines 13-32).

Regarding claims 65-68, 70-73, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present invention to apply the teachings of Majima into the method of BOI as both are related to the Art Unit: 2818

same subject matter of manufacturing a semiconductor device having a plurality of pixel electrodes with gaps/boundary portions therebetween formed in a matrix on the protection insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Regarding claims 74, 80, 86, 93, BOI, figures 2A, 2B, pages 1-3, disclose a method of manufacturing a semiconductor device comprising the steps of: forming electrodes 208, 209 over a substrate 205 having an insulating surface; forming stripped electrodes 208, 209 over a substrate 205; forming pixel electrodes 208, 209 that arte electrically connected to the respective semiconductor elements; forming semiconductor elements arranged in matrix form over a substrate 205.

BOI fails to teach forming a DLC film to cover the pixel electrodes; forming an insulating layer on the DLC film; planarizing the insulating layer so that a surface of the DLC film and a surface of the insulating layer become flush with each other, thereby filling boundary portions between the stripped/pixel electrodes with the insulating layer.

However, Majima, figures 1-8, and related text on col. 1-12, (figures 1, 3A-3D, col. 7, lines 15-50, col. 9, lines 60-67, col. 10, lines 1-32), teach the steps of forming a DLC film to cover the pixel electrodes; forming an insulating layer on the DLC film; planarizing the insulating layer so that a surface of the DLC film and a surface of the insulating layer become flush with each other, thereby filling boundary portions between the stripped/pixel electrodes with the insulating layer (see col. 10, lines 13-32).

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Regarding claims 75-79, 81-84, 87-92, 94-99, see BOI, pages 1-3, Majima, col. 1-12.

It would have been obvious to one having ordinary skill in the art at the time of the present

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invention to apply the teachings of Majima into the method of BOI as both are related to the

same subject matter of manufacturing a semiconductor device having a plurality of pixel

electrodes with gaps/boundary portions therebetween formed in a matrix on the protection

insulating layer, and a filler is formed so as to be at the same level as that of the surfaces of

the pixel electrodes. By this process, the surfaces of the pixel electrodes are made flush with

the surface of the filler filling the gaps and at the same time the surface of the pixel electrodes.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure: Matsubara'081, Hirakata'055, Hirakata'645 are cited as of interest.

4. A shortened statutory period for response to this action is set to expired 3 (three) months

from the date of this letter. Failure to respond within the period for response will cause the

application to become abandoned (see 710.02 (b)).

5. Any inquiry concerning this communication on earlier communications from the examiner

should be directed to David Nhu, (703) 306-5796. The examiner can normally be reached

on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be

reached on (703) 308-4910.

The fax phone number for the organization where this application or proceeding is assigned is

(703) 308-7382.

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Any inquiry of a general nature or relating to the status of this application or proceeding should

be directed to the receptionist whose telephone number is (703) 308-0956

David Nhu

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January 5, 2004

SwiRlan

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